SGS-THOMSON MICROELECTRONICS

DEMOBOARD

AUDIO - VIDEO

SUMMARY **Page**

1 - SUMMARY OF FEATURES

- 2 x SCART CONNECTORS
  SCART 1 : RGB + FB inputs, CVBS input, CVBS output (TV), Stereo audio inputs, stereo audio outputs
  SCART 2 : RGB + FB inputs, CVBS input, CVBS output, Stereo audio inputs, stereo audio outputs
- 2 x EXT CVBS (Cinch) connectors
  Ext CVBS IN, CVBS OUT (Picture In Picture)
- 4 x Stereo audio (Cinch) connectors
  Ext audio IN 1, Ext audio IN 2, Ext audio OUT TAPE OUT
- TV AV connections (internal connections)
  TV TUNER : CVBS input, STEREO AUDIO inputs
  To video processor : RGB + FB, Y/CVBS/SYNC, C/CVBS
  To audio processor : Stereo audio outputs
- MCU/PC INTERFACE

2 - INTRODUCTION

In recent years, the selection of hardware available for complete TV systems has grown considerably. Peripherals such as VCRs, laser disc players, camcorders, and home computers are now commonplace on the consumer market. Thus, modern TV receivers are required to control and route many signals between these external peripherals and various internal stages of the set. Therefore it is becoming a standard practise to feature many input and output connections at the rear of the unit (SCART, SVHS, RCA, etc...).

High-end TV sets have extra integrated features such as internal satellite decoders, 2 tuners, picture in picture, HIFI sound, multistandards reception, etc. with menu control of all functions via the remote control.

All these extra signal sources and functions must be handled at the audio/video matrix section of the TV set. The significance and complexity of this stage has been forced to grow in pace with these modern trends, and the use of a microprocessor for control is common place. In parallel with this, the physical size of the TV receiver chassis is required to be minimized. Thus, modern TV receiver designs challenge traditional methods of switching these signals in terms of both economy and technical performance (since it is obvious that a greater number of uncorrelated signals present at this stage produce greater unwanted interaction effects).

The technical performance requirements are further stressed by the evolution of techniques that are intended to enhance both picture and sound quality (SVHS and nicam for example), which require wider bandwidth and lower distortion signal handling.

Conventional designs based on discrete circuitry or low cost analog CMOS gates are no longer feesible. The market demand is thus for dedicated ICs with optimised performance for handling all the audio and video interconnections under direct microprocessor control.

SGS-THOMSON has answered the demands of the TV industry with the introduction of optimized audio and video matrix products that can be directly controlled by the I^2C bus. The high signal density, performance and flexibility of these components allow them to satisfy a wide range of applications.

3 - GENERAL DESCRIPTION/ARCHITECTURE

This demonstration board attempts to show the versatility, performance and simplicity of an audio/video matrix system that uses only three SGS-THOMSON ICs. The circuit architecture is intended to reflect a typical high-end TV set AV stage with SCART connections (with RGB inputs), SVHS inputs and outputs, internal and external CVBS and stereo audio connections.

Figure 2 shows a simplified circuit schematic of the demo board.

Two SCART sockets are incorporated which deliver two RGB and Fast Blanking signals which are switched by the TEA5116.

All audio connections are handled by the TEA6420 I^2C bus controlled audio matrix. Any of the 5 stereo audio sources can be routed to one or more of 4 stereo outputs with bus programmable gain (from 0 to 6 dB). All remaining video signal switching is performed by the TEA6415B I^2C bus controlled video matrix.

Two SVHS inputs are featured with corresponding audio inputs. The Y/C components connect to 4 of the TEA6415B inputs, and an SVHS output socket is included which can receive one of these Y/C sources. An extra EXT CVBS IN (BNC connection) is featured to complete the video matrix inputs. This function is useful for Y + C mix requirements (see applications section Figure 4). The video matrix outputs connect to the TV output (LUMA + CHROMA), SCART 2 CVBS out, SVHS output (LUMA + CHROMA), and an external CVBS OUT (BNC connection), which can be employed as the PIP output.

The audio matrix (TEA6420) handles all the peripheral stereo audio inputs plus the TV IF sound. Two pairs of outputs are connected by CINCH - one AUDIO OUT which is to be used in conjunction with SVHS OUT or CVBS OUT ; the other audio output pair is labelled TAPE OUT for direct sound recording or HIFI connection.

Figure 1 : AV Demoboard detailed Electric Schematic

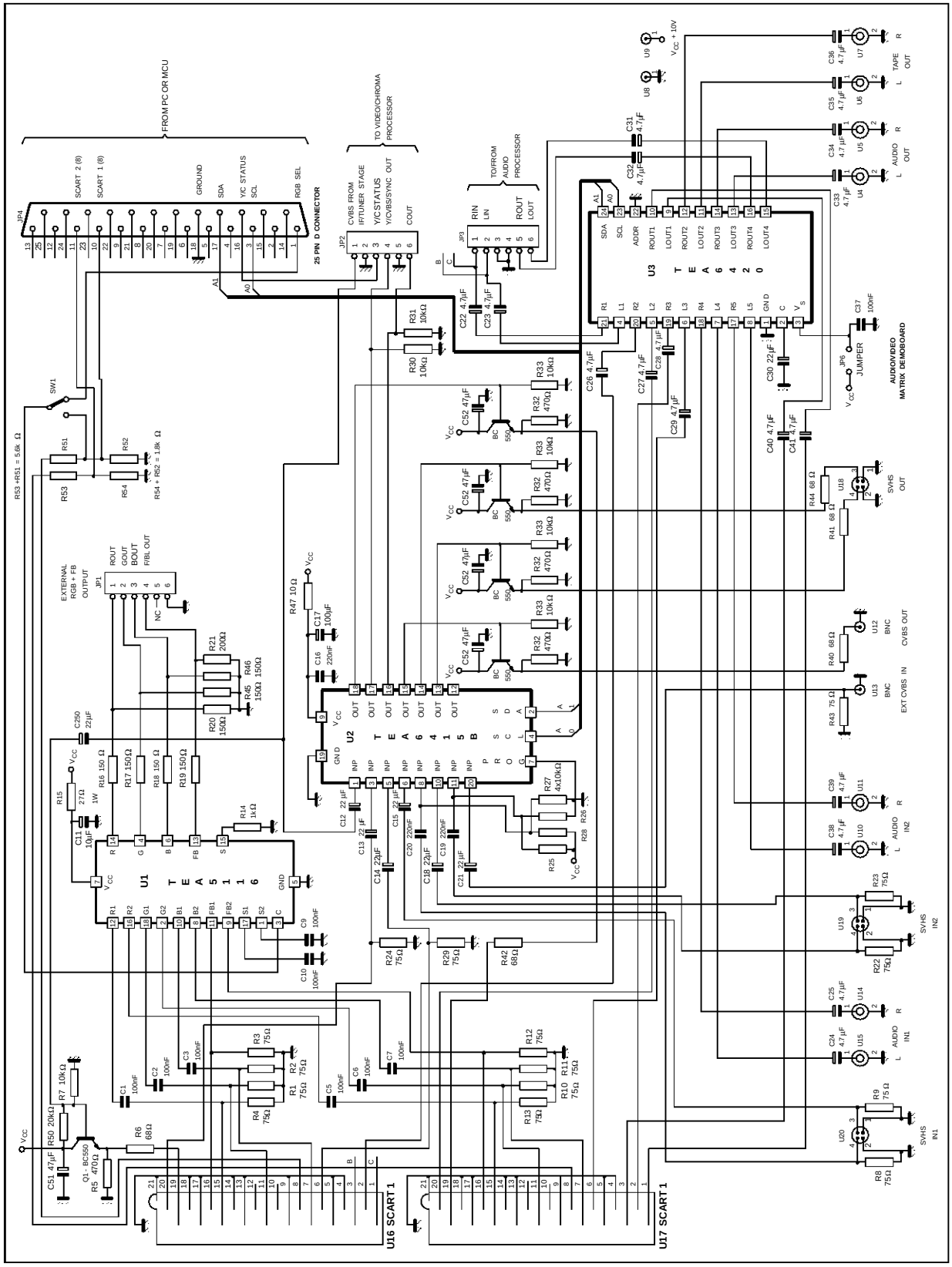
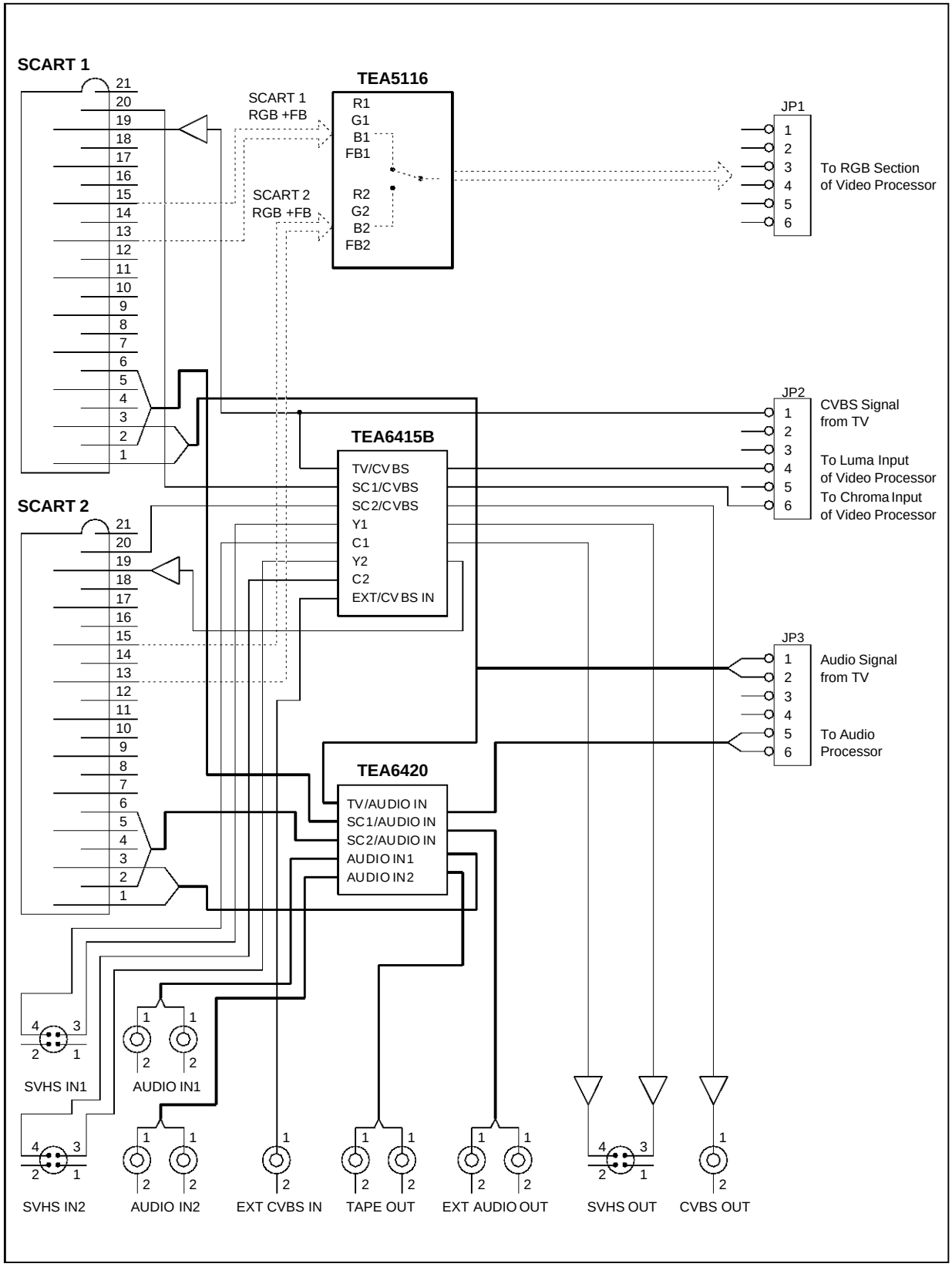


Figure 2 : Simplified AV Board Schematic



4 - APPLICATION

4.1 - TV Connections

Figure 3 shows the suggested method for connection of the AV Demo Board to the appropriate stages of a TV receiver.

4.1.a - AV board input signals from TV IF stage

The CVBS signal from the TV receiver's IF stage must be connected to the AV board at JP2 pin 1. The corresponding stereo audio signals are to be connected to JP3 pins 1 (stereo Right) and 2 (stereo Left).

4.1.b - AV board output signals to video/chroma processor

The AV board TV video output signals are connected on JP1 and JP2. JP1 has the RGB+Fb component outputs on pins 1,2,3, and 4 respectively. Usually, these signals connect directly to the video processor, since it has internal RGB switching to accommodate the external RGB source and TEXT RGB. However if this switching has to be performed externally to the video processor, an RGB+FB switch IC (TEA5114A or TEA5115) could be used. In this case, R21 should be increased to 300Ω.

JP2 connects the video matrix outputs to the TV. It must be noted that these signals are amplified (X2) at this point. Pin 4 must be connected to the luma signal processing circuit, and pin 6 to the chroma processing circuit. The total load impedance on the video matrix outputs must not be less than 3k, (note that characterisation was performed with the 10k loads supplied on the pcb). When the AV board is used in conjunction with the supplied PC software, a Y/C STATUS flag is output on pin 3. Three cases must be considered as follows :

(a) when an SVHS source is selected in the TV DISPLAY MENU, the Y signal is routed to JP2 pin 4 and the C signal to pin 6. The Y/C STATUS flag on pin 3 is a logic 0 in this case. The purpose of this function is to initiate control logic which can be used to bypass chroma traps (and consequently increase the luma bandwidth) when processing SVHS signals.

(b) when a CVBS source is selected, it appears at both outputs (pin 4 and pin 6). The Y/C STATUS is a logic 1 (+5V) in this case.

(c) when an RGB source is selected, the corresponding SYNC signal appears at both outputs (pin 4 and pin 6). The Y/C STATUS is a logic 1 (+5V) in this case also.

4.1.c - AV board outputs to audio processor

JP3 connects the stereo audio outputs to the TV audio processor.
Pin 5 is stereo Right and pin 6 is stereo Left.

4.1.d - AV board PICTURE IN PICTURE output

The CVBS OUT (BNC) can be employed for PIP applications. The demonstration software has a dedicated menu to select different CVBS sources for the PIP display.
Two SCART sockets are incorporated which deliver two RGB and Fast Blanking signals which are switched by the TEA5116.
All audio connections are handled by the TEA6420 I^2C bus controlled audio matrix. Any of the 5 stereo audio sources can be routed to one or more of 4 stereo outputs with bus programmable gain from (0 to 6dB). All remaining video signal switching is performed by the TEA6415B I^2C bus controlled video matrix.

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Figure 3 : AV Demoboard Connections to TV Receiver

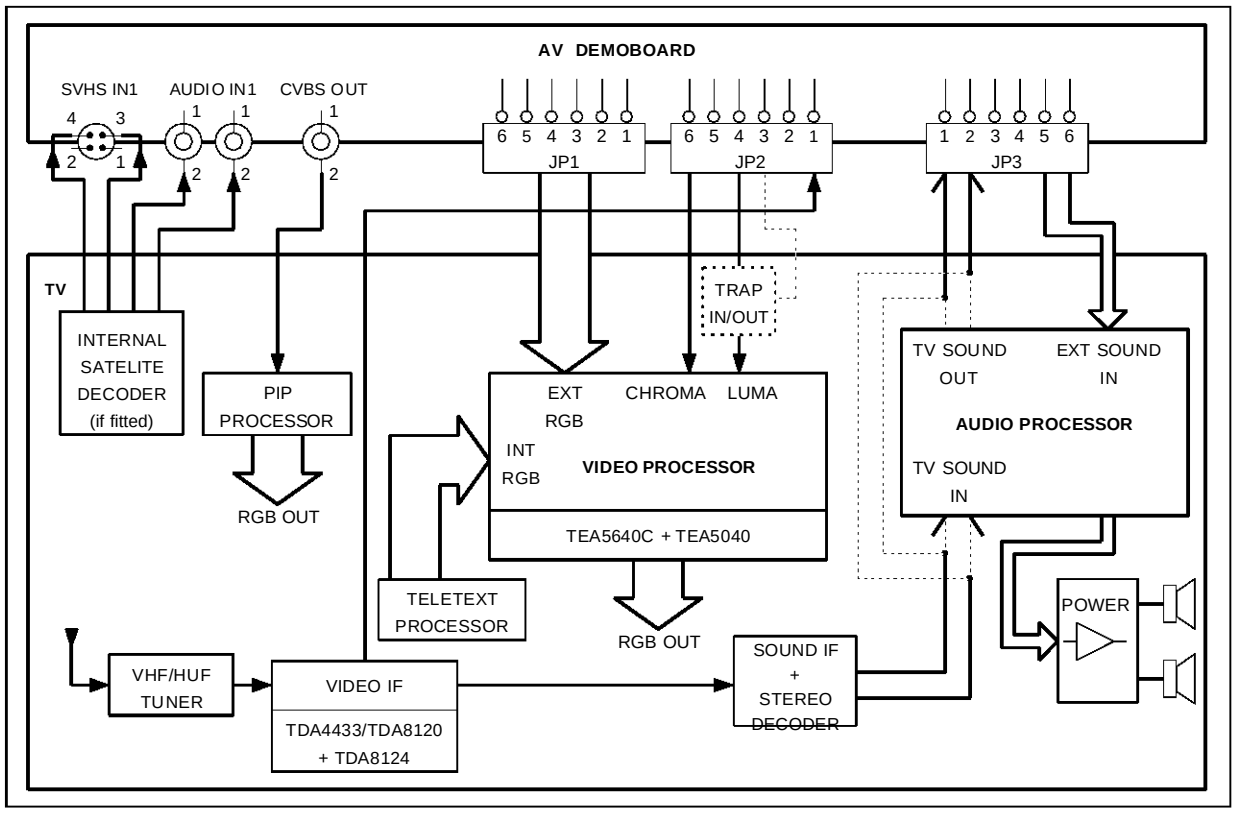
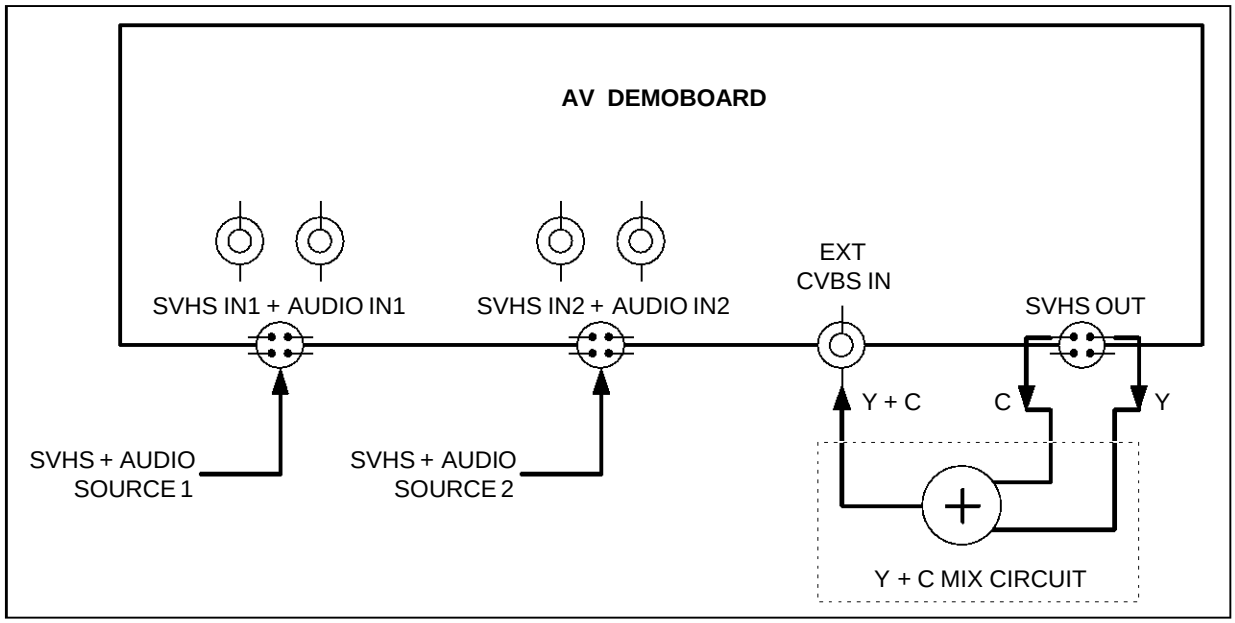


Figure 4 : Suggested Method for Y + C Mixing Function



4.2 - External Inputs and Outputs

4.2.a - Scart

SCART 1 obeys the norms concerning its CVBS output (pin 19) and the stereo audio outputs (pins 1 and 3), i.e. the TV tuner/IF CVBS signal and corresponding audio signals are sent directly to the SCART 1 outputs. This facility allows connection to a VCR or payTV decoder for example. The CVBS and audio input signals are directed to the matrix inputs.

Both SCART connections have their pin 8 signals connected to the MCU connector (JP4) to allow the micro to initiate the automatic switching function (see below). Also, the RGB switching can be initiated automatically from the SCART 1 pin 8 signal by positioning SW1 to the junction of R51 and R52.

4.2.b - SVHS

Two external SVHS sources can be connected to the AV board. Alternatively, SVHS IN1 (and AUDIO IN1) can be employed to connect a satelite decoder if fitted.

Quite often there is a requirement to mix the Y and C components of the connected SVHS devices. This function is almost invariably required in applications that feature the PIP facility. Figure 4 illustrates how the AV demo board can fulfill this requirement by using SVHS OUT and EXT CVBS IN to interface to an external Y + C mixing circuit. This is an economical way to perform this function since only one mixing circuit is required to serve two separate SVHS inputs.

The video matrix (TEA6415B) under I2C control selects the SVHS source to be mixed and at the same time routes this (Y+C) signal to the required output (or outputs) i.e. SCART 2 and/or CVBS OUT (PIP).

Note that the demonstration software does not perform this function automatically, but can simulate this by appropriate selection within the PIP DISPLAY SELECT or SCART 2 OUTPUT SELECT MENU (ie. EXT CVBS IN selected) and then the appropiate selection of input source within the SVHS OUT SELECT MENU.

4.3 - MCU/PC Interface

The AV demo board has a 25 pin "D" connector to provide connection to a PC or microprocessor for control.

The MCU controls all switching functions by delivering serial I^2C bus signals (SDA + SCL), with the exception of the RGB source selection which is controlled by a single input (JP4 pin 1) or SCART 1 pin 8.

Both SCART pin 8 signals are sent to the MCU connector (JP4) for status or detection functions. When used with the demonstration software, this information is used to generate the automatic switching function. Note that if both SCARTs are activated, SCART 1 is given priority. More detailed information on the operation of the supplied controlling software can be seen in the AV DEMO BOARD SOFTWARE USER GUIDE.

A detailed description of the demonstration software is available on request. It provides both :

- useful *information for software development when using a microprocessor* (PC Software - User Guide)
- *essential information for modification of the existing program (in C language)* (PC Software - Analysis)

After power-up, the AV board configuration is indeterminate. Therefore, an initialisation routine must be performed when developing the controlling software. This requires a total of 10 16-bit words. The first byte of each word consists of the unique chip address for the TEA6415B or TEA6420, the second byte being the necessary data for the required connection.

A suggested initialisation routine is shown in Table 1.

Table 1 : AV Board Initialisation Routine

Word	1st Byte (chip address)		2nd Byte (data)		
1	1000	0110	0000	0011	
2	"	"	0000	1011	
3	"	"	0001	0011	TEA6415B Initialisation
4	"	"	0001	1011	
5	"	"	0010	1100	
6	"	"	0010	0001	
7	1001	1000	0001	1000	
8	"	"	0011	1000	TEA6420 Initialisation
9	"	"	0101	1011	
10	"	"	0111	1000	

The initialisation procedure consists of 6 words for setting up the video matrix (ADDRESS = 86 (HEX)), and a further 4 words for setting up the audio matrix (ADDRESS = 98 (HEX)). The set up configuration programmed is as follows:

(1) The TV CVBS input signal is sent to all outputs except SVHS OUT, which receives SVHS IN 1 Y and C connections.

(2) The TV audio input is routed to all audio outputs except EXT AUDIO OUT which is connected to AUDIO IN 1.
A gain of 0 dB is set for all audio outputs.

Note that this configuration is programmed by the supplied software when first installed and also when the <RESET> function is selected.

All subsequent configurations are made by issuing 16 bit words for video matrix setup, and for the appropriate corresponding audio matrix setup. Table 2 shows the required 2nd byte of transmission for the various AV board configurations.

Table 2 : AV Board Configuration table (2nd Byte of Transmission)

OUTPUT SELECTION			
VIDEO MATRIX		**AUDIO MATRIX**	
00001XXX	Y/CVBS/SYNC (OUT)	011G1G0XXX	Audio out (TV)
00010XXX	C(OUT) (TV)		
00000XXX	SCART2 CVBS (OUT)	000G1G0XXX	SCART2 audio out
00100XXX	Y SVHS OUT	010G1G0XXX	Ext. audio out
00101XXX	C SVHS OUT		
00011XXX	CVBS (OUT)	001G1G0XXX	Tape out
INPUT SELECTION			
00XXX011	TV CVBS IN	0XXG1Go000	TV audio in
00XXX010	SCART1 CVBS IN	0XXG1Go001	SCART1 Audio in
00XXX000	SCART2 CVBS IN	0XXG1Go010	SCART 2 audio in
00XXX001	Y_1 SVHS IN 1	0XXG1Go011	Audio In 1
00XXX100	C_1 SVHS IN 1		
00XXX101	Y_2 SVHS IN 2	0XXG1Go100	Audio In 2
00XXX111	Y_2 SVHS IN 2		
00XXX110	EXT CVBS IN		
		0XXG1Go101	Audio mute

Note : G1 and Go set the audio gain as shown below :

G1	Go	GAIN
0	0	6 dB
0	1	4 dB
1	0	2 dB
1	1	0 dB

5 - TYPICAL ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
SUPPLY			
V_{CC}	Supply Voltage	10	V
I_{CC}	Supply Current (all outputs driven)	260	mA
RGB SECTION			
	Bandwidth (V_{RGB} = 0.7V_{PP}, see FIgure 5)	29	MHz
	Crosstalk f_{RGB} = 1MHz f_{RGB} = 5MHz	-61 -51	dB dB
	Output D.C. Level	0.9	V
VIDEO SECTION (CVBS)			
	Bandwidth (V_{IN} = 1V_{PP}, see Figure 6)	15	MHz
	Crosstalk (f_{IN} = 5MHz, see Figure 7)	-56	dB
	Output Gain TV video outputs Other video outputs - when terminated	6.5 0.5	dB dB
	Output D.C. Level TV video outputs Other video outputs - when terminated	3.2 1.25	V V
VIDEO SECTION (SVHS)			
	Bandwidth (V_{IN} = 1V_{PP}, see Figure 6)	15	MHz
	Crosstalk (f_{IN} = 5MHz)	-52	dB
	Output Gain (when terminated)	+0.5	dB
	Output D.C. Level (when terminated)	1.25	V

5 - TYPICAL ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Value	Unit
AUDIO SECTION			
	Bandwidth (V_{IN} = 1V_{RMS}, Gain = 0dB, see Figure 8)	630	kHz
	Crosstalk (V_{IN} = 1V_{RMS}, f_{IN} = 1kHz)	-96	dB
	Supply Rejection (f = 1kHz, V = 0.5V_{PP})	-80	dB
	Signal to Noise Ratio	100	dB
	THD V_{IN} = 1V_{RMS}, f_{IN} = 1kHz, Gain = 0dB V_{IN} = 1V_{RMS}, f_{IN} = 20Hz to 20kHz, Gain = 0dB V_{IN} = 0.5V_{RMS}, f_{IN} = 1kHz, Gain = 6dB	 0.005 0.008 0.04	 % %
MISCELLANEOUS			
	Crosstalk between RGB and VIDEO Sections (f_{IN} = 5MHz)	-65	dB
	Crosstalk between CVBS and SVHS Sections (f_{IN} = 5MHz)	-51	dB

Figure 5 : RGB -3dB Bandwidth Typical Characteristics

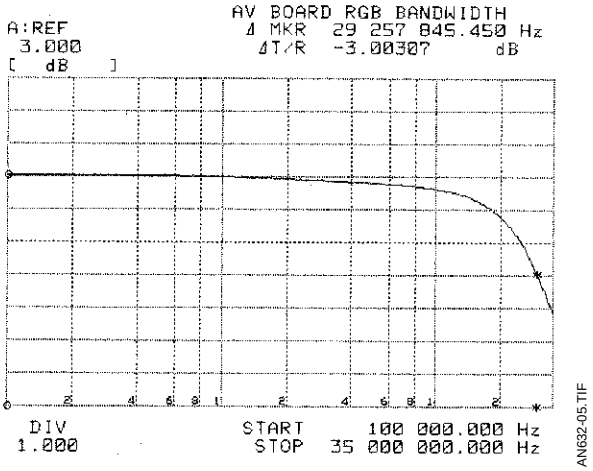


Figure 6 : Video -3dB Bandwidth Typical Characteristics

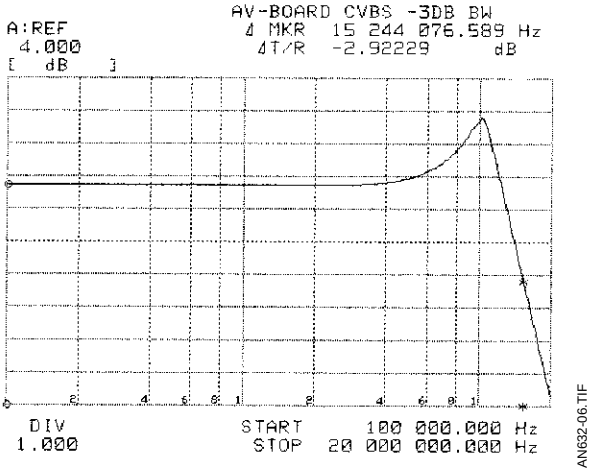


Figure 7 : Video Crosstalk Typical Characteristic

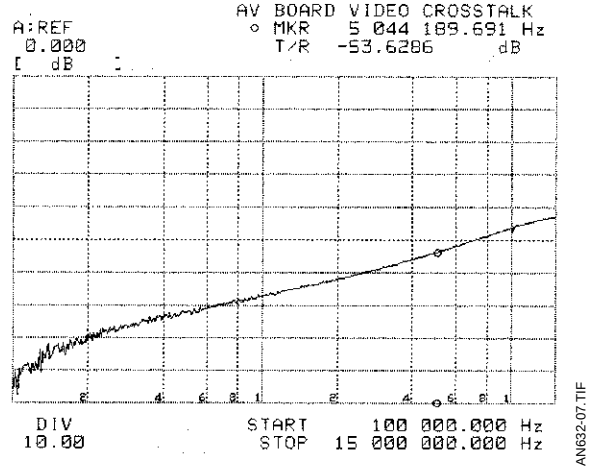
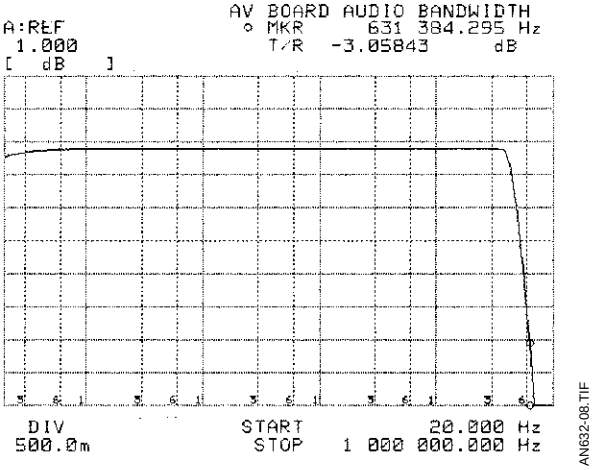


Figure 8 : Audio -3dB Bnadwidth Typical Characteristic



6 - DESIGNING WITH AUDIO/VIDEO SWITCHES & MATRICES

The true matrix nature of the TEA6415B and TEA6420 allow greater design flexibility. Since TV receiver AV stage architectures vary from design to design, a specific dedicated ic approach can often restrict the designers capacity. Therefore the flexibility of these components allow them to be considered as building blocks for AV stages, whilst having optimised performance and signal processing.

Both devices have the option of two different I^2C addresses which can be programmed by a voltage on the ADDR pin. This facilitates employment of more than one device on the same bus to provide more inputs and/or outputs if required.

To further add to its versatility, the TEA6415B can switch composite (CVBS), luma (Y), or sync signals, with aligment of the bottom of the sync pulse to a fixed clamping level, or can also be used to switch other signals such as chroma (of an SVHS source) and MAC signals. For the latter cases, it is necessary to remove the internal clamping arrangement to avoid signal clipping. This can be accomplished by biasing, the signal to a sufficient D.C. level with a simple resistor divider. For optimum dynamic range, it is recommended to pull-up to around $V_{CC}/2$.

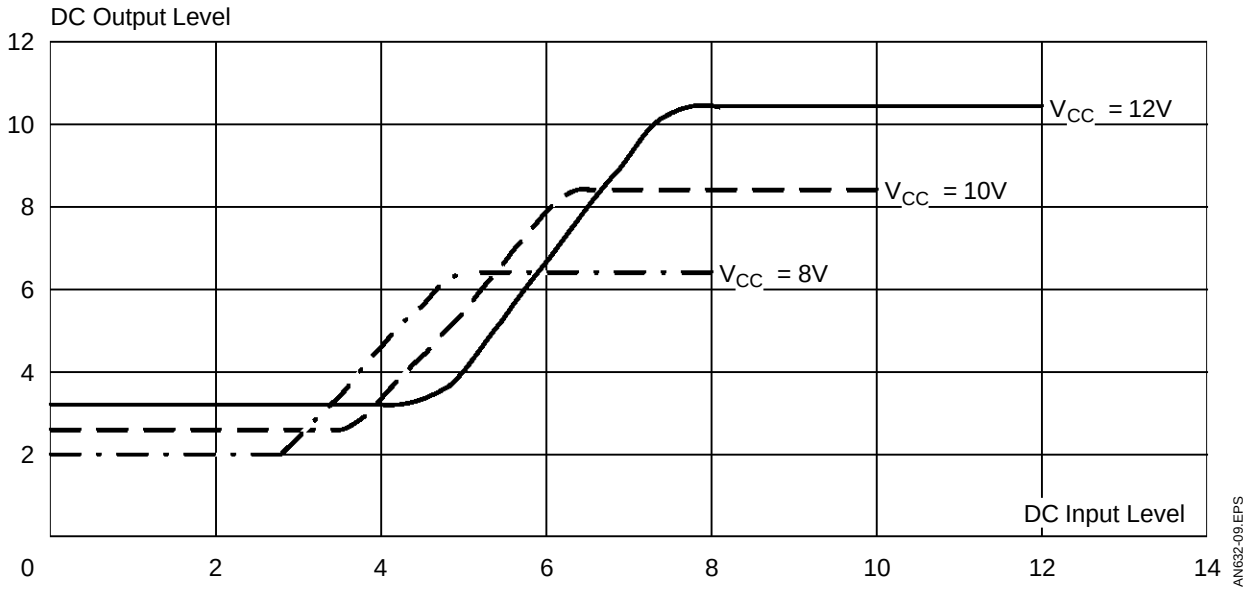
Figure 9 shows the range of unclamped signal measured on a typical device, and illustrates the optimum biasing point.

Note that the TEA6415B adds 6.5dB gain and should thus be taken into account for unclamped input signal range to avoid output signal clipping.

Neither device is intended to drive low impedances. Therefore, in situations where 75Ω has to be driven, for example, an external buffer is required. This need only be a simple and inexpensive transistor follower. The nominal load on the video matrix outputs should be 10kΩ, and not less than around 3kΩ. For the audio matrix, the minimum output load resistance is 2kΩ.

Considering crosstalk performance, the impedance of the signal sources must be sufficiently low. Therefore, when an input is not used in the application, it must be bypassed to ground with a 220nF capacitor in the case of video switches and matrices, and 4.7µF in the case of the audio matrix to ensure good crosstalk rejection performance.

Figure 9 : Typical Unclamped Signal Range



6.1 - Performance Optimisation by PCB Layout

The application of integrated circuits designed for video signal manipulation does not necessarily ensure adequate circuit performance. Although, care is taken to optimise the performance of the IC by design, when implemented on a badly configured circuit board, the performance can be less than satisfactory.

At higher frequencies, parasitic elements on the pcb cause signals to radiate to other parts of the circuits. The control of this signal crosstalk effect is of paramount importance in the design of audio/video stage circuits, since a concentration of uncorrelated signals occurs mainly at this region of the chassis.

Good HF layout techniques must be used when designing the pcb.

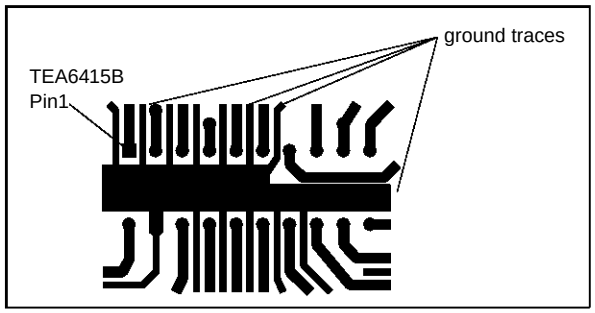
Some general rules for guidance are as follows :

6.1.a - Ground Layout

Extensive and appropriate grounding is of singular importance. Ground layout can effictively reduce capacitive signal crosstalk by providing a preferential low impedance path for radiated signals. On the other hand, the ground traces themselves can become the source of the signal crosstalk in certain situations. We can consider two cases of crosstalk by ground layout:

(a) At the switch or matrix ic connection; the signal crosstalk can be considered as mainly due to capacitance, and thus extensive ground layout should be employed to shield adjacent inputs or outputs using a comb-like configuration as shown in the TEA6415B ic footprint layout example of Figure 10.
The interpin ground traces should extend out from the IC footprint to maintain the shielding right to the signal source connection to the pcb. This method should be adopted for any regions of concentrations of signals (such as scart connectors for example).

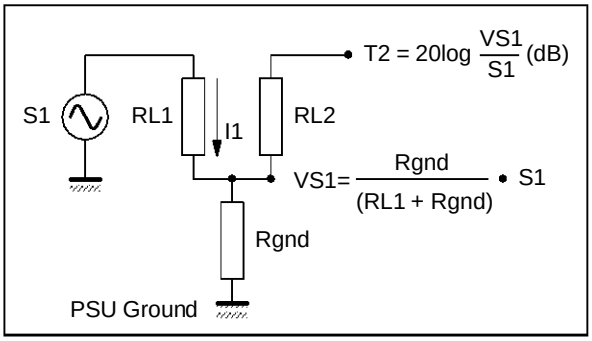
Figure 10 : TEA6415B IC footprint ground layout



(b) At the signal (input or output) terminations, or where low impedances are driven (in the case of the RGB outputs of RGB switching ics - TEA5114A, TEA5115, and TEA5116 for example) ; the signal crosstalk is resistive and is normally coupled via the ground traces themselves.

Briefly, this effect is caused by the relatively large signal currents flowing to ground at low inpedance terminations in the circuit. The small amounts of ground path resistance are sufficient to superimpose this signal on the grounded side of another signal's termination resistor as illustrated in Figure 11.

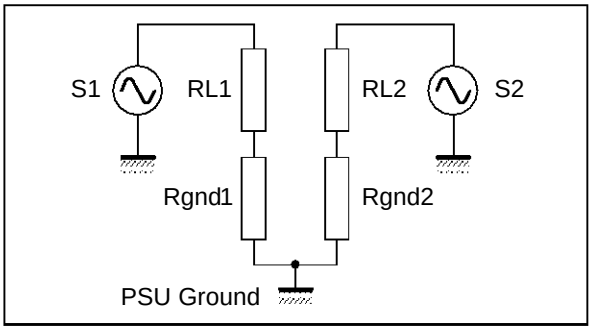
Figure 11 : Ground path induced signal crosstalk



This type of crosstalk effect can be minimised by using a different type of ground layout at these areas of the pcb known as "star connection", and is shown in Figure 12.

This method involves employing unique ground traces for low impedance terminations which are joined together only at the psu ground terminal.

Figure 12 : Star Connected Ground Layout Method



6.1.b - Signal Paths

Signal traces should be kept as short as practically possible, ie. the switching IC should be placed as close as possible to the signal input connectors (scart, RCA external inputs, SVHS inputs, connection of signal from the tuner/IF stage, etc.).

6.1.c - Component Type and Orientation

For A.C. coupling video signals, it is important to select an appropriate type and value capacitor. For example, for chroma signals (that do not have lower frequency synchronisation components) a 220nF polyester or multilayer ceramic capacitor is best, whilst a CVBS (or Y) signal would usually require a much higher value (10 to 22µF) electrolitic capacitor.

A low profile circuit design is better than vertical component orientation. The use of IC sockets (although offering easy circuit maintenance) degrades the performance and should thus also be avoided. A surface mounted component layout gives the best performance of all.

6.2 - Performance Optimisation by Circuit Design

It has already been stated that source and load impedances play a significant role in the circuit performance. The switch and matrix devices have been designed to operate sufficiently in normal circuit architures without the need to modify the defined impedances.

It must be reminded that psu decoupling is essential at any node where signal related supply currents will flow such as V_{CC} pins of ICs, and the collectors of transistor followers used for driving loads. Again the type and value of capacitor used is important. Best video performance is achieved when power supplies are decoupled with a high value electrolytic or tantalum bead capacitor in the range 10 to 47µF, connected in parallel with a much lower value polyester or multilayer ceramic type in the range of 100 to 220nF. Further psu decoupling improvment can be achieved by connecting a series resistance in the psu connection just before the decoupling capacitors (which must be mounted as close to the devices V_{CC} pin as possible) of a suitably low value so as not cause any significant voltage drop (in the region of 10 to 50Ω for example).

The implementation of a series resistor in the input signal path (after the coupling capacitor) to the TEA6415B can occasionaly offer improved crosstalk rejection. The optimum value of resistor will be largely dependant on the pcb parasitic capacitances.

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